IN THE SPECIFICATION:

Please revise the specification as follows:

Please amend paragraph number [0001] as follows:

[0001] This application is a division of U.S. patent application serial no. 09/457,155, filed December 8, 1999, which has issued as U.S. Patent No. 6,708,248 on March 16, 2004, and claims priority on U.S. Provisional Application No. 60/145,222, filed July 23, 1999, both of which are hereby incorporated by reference.

Please amend paragraph number [0005] as follows:

[0005] In the memory system shown in Fig. 2, a single [[64]] 64-bit line, data bus is shared by four 64-bit memory devices. In the example shown in Fig 1, accessing four 64-bit memory devices would require a 256 line wide data bus. Thus, the structure of the memory system shown in Fig 2 represents an advance over that of Fig. 1. However, the reduction in relative data bus width comes with some additional overhead. In the memory system of Fig. 2, each memory device receives an individual set of control signals 14 from memory controller 10. These separately transmitted signals are required to regulate memory device access to the common data bus lines.

Please amend paragraph number [0010] as follows:

[0010] Thus, in one aspect, the present invention provides a memory system operating in either a first mode or a second mode of operation. ~~and comprising;~~ The memory system includes a memory controller is connected to memory devices via at least one channel[[,]]. The ~~the~~ memory controller communicates~~ing~~ at least one command to each one of memory devices via the at least one channel[[,]]. ~~such that while~~ While the memory system operates in the first mode, one of the memory devices responds to the at least one command to accomplish transfer of data between the one memory device and the memory controller during a first time period[[;]]. ~~and while~~ And while the memory system operates in the second mode, a plurality of the memory devices responds to the at least one command to accomplish transfer of data between the plurality of memory devices and the memory controller during the first time period.

Please amend paragraph number [0011] as follows:

[0011] In another aspect, the present invention provides a memory system operating in either a first mode or a second mode of operation. ~~and comprising;~~ [[a]] The memory system includes a memory controller that is connected to memory devices via at least one channel[[,]]. The ~~the~~ memory controller communicates~~ing~~ at least one command to each one of memory devices via the at least one channel[[;]]. ~~such that~~ While ~~while~~ the memory system operates in the first mode, one of the memory devices responds to the at least one command to change operating states[[,]]. ~~and~~ And while the memory system operates in the second mode, a plurality of the memory devices responds to the at least one command to change operating states.

Please amend paragraph number [0013] as follows:

[0012] Thus, in one aspect, the present invention provides a memory system ~~comprising;~~ including a memory controller connected to at least one channel, and memory devices connected to the at least one channel[[,]]. ~~wherein at~~ At least one of the memory devices is a low bandwidth device being individually incapable of communicating a first data block with the memory controller during a first time period[[,]]. ~~wherein the~~ The memory controller communicates control information to at least a first plurality of the memory devices via the at least one channel, and in response to the control information, the first plurality of memory devices, as a multiplexed group on the channel, communicates a first data block between the memory controller and the first plurality of the memory devices during a first time period.

Please amend paragraph number [0014] as follows:

[0013] In still another aspect, the present invention provides a memory system ~~comprising;~~ including a memory controller connected to at least one repeater via a main channel[[,]]. ~~wherein each~~ Each repeater connects a first plurality of memory devices via at least one auxiliary channel.~~, and wherein each~~ Each one of the first plurality of memory devices is a low bandwidth device individually incapable of communicating a first data block with the memory controller during a first time period[[,]]. ~~and wherein the~~ The memory controller communicates control information to the first plurality of the memory devices via the at least the main channel, the at least one repeater, and the at least one auxiliary channel[[,]]. ~~and in~~ In response to the control information, the first plurality of memory devices, as a multiplexed group on the channel, communicates a first data block between the memory controller and the first plurality of the memory devices during a first time period.

Please amend paragraph number [0015] as follows:

[0014] In a related aspect to the foregoing, the present invention provides a memory system capable of selectively operating in first and second modes. ~~comprising;~~ The memory system includes a memory controller, memory devices, and a channel connecting the memory controller with the memory devices.~~, wherein each~~ Each one of the memory devices is capable of operating in at least a first and a second power state[[,]]. ~~the~~ The first power state consume~~sing~~ more power than the second power state, such that while the memory system is operating in the first mode, the memory controller generates a first power down device identification (ID) unique to one of the memory devices.~~, whereby the~~ The one memory device upon receiving the first power down device ID will transition from the first power state to the second power state[[,]]. ~~and while~~ And while the memory system is operating in the second mode, the memory controller generates a second power down device ID having the same structure as the first power down device ID, such that a plurality of memory devices upon receiving the second power down device ID transition from the first power state to a second power state.

Please amend paragraph number [0016] as follows:

[0015] In another related aspect, the present invention provides a memory system ~~comprising;~~ including a memory controller connected to a data bus. ~~comprising~~ The data bus includes a plurality of lines. ~~and generating~~ The memory controller generates one or more command packets[[,]]. The memory system also includes a group of memory devices,

wherein each memory device in the group is connected to at least one of the plurality of lines[[,]]. And each one of the memory devices in the group comprising includes a circuit responsive to the one or more command packets from the memory controller, such that the group of memory devices combine to output a first data packet during a first time period by multiplexing data onto the data bus during the first time period.

Please amend paragraph number [0017] as follows:

[0016] In still another related aspect, the present invention provides a method of reading data in a memory system during a first time period[[,]]. the The memory system comprising includes a memory controller connected to memory devices via a data bus having multiple data bus lines[[,]]. the The method comprising; includes communicating at least one command packet from the memory controller to a plurality of the memory devices, for each memory device in the plurality of memory devices, and seizing at least one data bus line during the first time period and returning data to the memory controller via the at least one data bus line in response to the at least one command packet.

Please amend paragraph number [0018] as follows:

[0017] In still another related aspect, the present invention provides a method of reading a first block of data in a memory system during a first time period[[,]]. the The memory system comprising includes a memory controller connected to memory devices via a data bus having multiple data bus lines[[,]]. the The first time period comprising includes a sequence of second time periods.; and the The method comprising; includes communicating at least one command packet from the memory controller to a plurality of the memory devices, during each second time period, and outputting a second block of data smaller than the first block of data from a selected memory device in the plurality of memory devices via the data bus, such that a combination of the second blocks output during the first time period comprises the first data block.

Please amend paragraph number [0092] as follows:

[0092] When the memory system is operating in chip-kill mode, syndrome for a first data block can be distributed among the second data blocks read from each one of the plurality of memory devices. The exact form of such syndrome distribution is left to the memory system designer. Syndrome may be evenly spread across a group of second data blocks, or some second data blocks may be entirely made up of syndrome. During the four

clock cycle period of time, a complete 16-byte data packet is returned to the memory controller. That is, the 16 bytes forming the data packet are returned two bytes per half clock cycle from each of eight memory device during this time period. The data packet returned to the memory controller in chip-kill mode has the same number of bytes as the data packet returned in non-chip-kill mode. Further, the data packet returned in chip-kill mode is transmitted over the same structure and using the same data packet transfer timing as those used in non-chip-kill mode. The additional timing mechanism required to sequentially read a series of second data blocks from the plurality of memory devices in order to form the first data block is discussed in commonly assigned U.S. Patent ~~Application No. 09/395,160~~ No. 6,370,668, with reference to the ROW and COL command packets used in chip-kill mode.